# Final project report: Mixed analog and digital integrated circuits

**Project leaders**
*Prof. Mark Vesterbacka, Linköping University*
*Dr. J. Jacob Wikner, Infineon Technologies AB*

**Duration**
The project started 1 Jan. 1999, and ended 31 Dec. 2004.

**Research area**
The current trend within electronics research is to solve problems related to System-on-Chip (SoC), where the ultimate goal is to put all electronics in a product on a single silicon chip. Achieving this goal would significantly reduce cost and power consumption of a product, while the reliability and performance would increase. With the rapidly increasing integration of circuits on silicon chips already taking place, there are mainly two major problems remaining that need to be addressed. One problem is to handle the complexity within the design of large systems. The other problem is to integrate analog and digital circuits on the same chip. In this project we have mainly focused on the latter problem.

**Major achievements**

The main achievement during the first year (1999) was the invention of a new method to interface the digital parts to the analog synthesizer in a digital-to-analog (DA) converter [3, 4, 6]. Use of this method reduces the glitch noise, which is a serious problem in high-speed or oversampling DA converters. Prior methods aiming at solving this particular problem has all suffered from that the design complexity becomes unmanageable for high resolutions (e.g. 10-bit DA converters). Our method does not suffer from this. It should be appropriate for, e.g., 14-bit high-speed DA converters. This invention resulted in a patent [42].

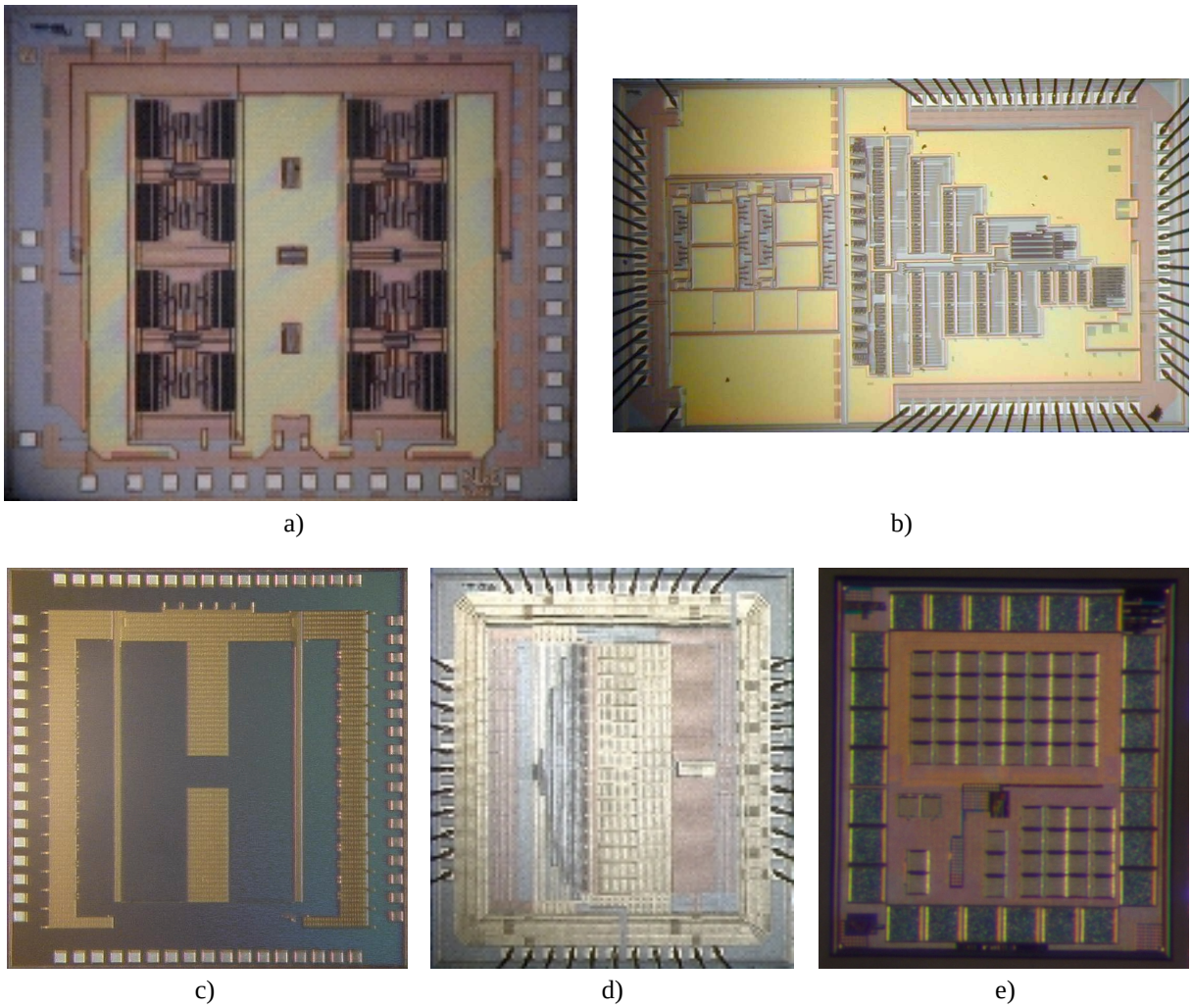
During the second year (2000) we have developed an encoding algorithm for the method above. The hardware has been designed for a 14-bit encoder, which seems to be sufficiently small for practical use [10]. Also, several ideas have come up as "side effects" from the approach above. One of the new ideas uses a special coding to reduce errors induced in the analog domain with digital signal processing [8, 9]. This invention did also lead to a patent [44].

During the third project year (2001) we have developed our invention from 1999 so that the glitch noise spectrum is shaped to yield a low relative error [12]. Comparing with prior methods, the results indicate a significant improvement in the relative error. We have also made improvements to the hardware for the encoding algorithm. As a "side effect" of this work we have demonstrated a new square root approximation technique with less latency than prior methods. A very interesting result is that we have been able to extend this technique to implementation of fast division [36], which so far generally has been avoided in DSP hardware due to the long computational latency. We evaluated a technique for enhanced static performance of DA converters and obtained good results from measurements of a test chip, shown in Fig. 1 a). We did also perform simulations that showed limited efficiency of using the technique in the presence of dominating dynamic errors [14, 20].

During the fourth project year (2002), project leader M. Vesterbacka became full professor in Electronics Systems, and the first licentiate thesis was presented in Nov. [21]. We have designed a mixed-signal test circuit consisting of an analog filter used for estimating analog performance and a digital filter block for which a number of parameters can be controlled [16, 19, 23]. With this experiment we are able to evaluate the effect of digital noise injected into the analog parts in an actual implementation [25, 28, 34], and how different techniques reduce the noise. A photograph of the fabricated test circuit is shown in Fig. 1 b). We have also designed a second chip with two on-chip DA-converters that can be configured into a number of experiments involving signal processing to improve the performance [15], Fig. 1 c). A study on mixed-signal circuits implemented in silicon-on-insulator (SOI) technology [26] was initiated during the second half of 2002.

During the fifth year (2003), a new method of coding the control signals in DA converters aiming at low glitches and high linearity was developed. A test chip for evaluation of the new code was developed and has since then been measured [27, 29, 32]. The new code performance yields similarly good performance as the invention from 1999, but with a considerably lower complexity of the required encoding hardware. The chip photograph is shown in Fig. 1 d). Other work performed is the characterization of the noise injection test chip above where the digital part has been fully characterized and we are currently finalizing the characterization of the analog part. Our first circuit implemented in SOI technology, a high speed comparator, was designed.

During the sixth and final project year (2004), the SOI comparator was manufactured and measured, which in large worked as expected [33]. The chip is shown in Fig. 1 e). This circuit was used as the base for the design of two different 6-bit flash AD converters in SOI technology. The first design employs a new, fast type of digital decoder that should obtain a sampling frequency above 1 GHz [31, 35]. The second design includes an innovative control of the voltage reference that will linearize the transfer characteristics of the converter [31]. The designs have been completed and will be manufactured during early 2005. During the spring 2005, the first dissertation within the project will be defended, as well as the second licentiate thesis.



a) b) c) d) e)

*Fig. 1. Chips manufactured during the project:*

*a) 14-bit DA converter with 40 MSamples/s conversion speed using a special linearization technique,*
*b) test chip for evaluation of the effect of digital noise injected into analog circuits,*
*c) dual 14-bit DA converter for on-line calibration improving the dynamic performance,*
*d) 12-bit reconfigurable DA converter employing a new coding technique, and*
*e) comparator for use in a future 1 GHz, 6-bit flash ADC, implemented in a new type of technology.*

**Research group**

A stated long-term goal with this project was to create a strong research group within the area of mixed-signal circuits. During the project time, the group has developed to currently include seven members. Besides the project leaders the group we have an industrial mentor, Dr. Mikael Rudberg, whom also have participated in our research projects [8, 9, 47], and the four graduate students Lic.Eng. K. Ola Andersson [1, 7, 11, 14, 15, 17, 18, 20, 21, 22, 27, 29, 30, 31, 32, 38, 40, 42], M.Sc. Niklas U. Andersson [2, 5, 8, 9, 11, 14, 15, 17, 18, 20, 21, 22, 44], M.Sc. Erik Backenius [16, 19, 23, 25, 28, 34], and M.Sc. Erik Säll [24, 26, 30, 31, 33, 35]. The group has supervised and examined about 60 final projects, approximately equally distributed on master and bachelor thesis works. Nine of the master theses were directly related to this project.

**Cooperation**

During the project, we have had good contact with Ericsson Microelectronics, which supported the continued project participation of leader Dr. J.J. Wikner and Dr. student N.U. Andersson after they had been employed by the company. Ericsson Microelectronics became a part of Infineon Technologies in 2002. Our cooperation has included project discussions, design reviews, and we have also been able to use Infineon's measurement laboratory for measuring our fabricated chips. While the actual designs carried out within the project has not been used in products, the ideas and concepts developed in the project have been integrated into the design flow at the Linköping branch of Infineon Technologies. We have also planned a common project where our group should investigate the substrate noise of some Infineon designs. Besides the cooperation with Infineon, we have also supervised a number of final projects for the companies Aerotech Telub, Ericsson Access, Ericsson Microelectronics, Ericsson Mobile Communications, Epact Technology, Image Systems, Sectra, SiCon, the Swedish Defence Research Agency (FOI), and Zarlink Semiconductor.

Within CENIIT we have recently had discussions on cooperating with the new CENIIT-project 04.07 *Flexible Frequency-band Reallocation* managed by Dr. P. Löwenborg, ISY. A possible outcome of the future cooperation would be research on how to improve the performance of AD converters with signal processing by exploiting new inventions and findings.

**Support**

During the project time we have received a total of 2 890 kSEK in financial support from CENIIT. Approximately 40% of this amount was spent on partially financing the salary of the project leader M. Vesterbacka, 30% was used to support the salary of Dr. student K. O. Andersson, and 6% was spent on design support contributions by "ammanuens" P. Lander, Dr. student E. Hjalmarsson, and research engineer G. Karlströms. The remaining 24% was used for costs like travel, copying, telephone, and other costs common to the department of Electrical Engineering.

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